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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,165	11/04/2003	Pierre Morin	02GR109854488	5541

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,165	MORIN ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/7/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-18 drawn to a semiconductor device in Paper No. 8 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 12, 14-16, 19-20 and 22-25 are rejected under 35 U.S.C. 102(e) as being anticipated by En et al., US patent No. 6,573,172.

Regarding claim 12, En teaches (fig. 2I) a semiconductor device comprising: a semiconductor substrate (106); at least one first MOS transistor (102) and at least one second MOS transistor (104) in the semiconductor substrate; a dielectric layer (172) on the at least one first MOS transistor (102) and on the at least one second MOS transistor (104); a first layer (150) covering the at least one first MOS transistor (102) and having a first residual stress level (refer to col. 7, lines 50-60); and a second layer (130 and 140) covering the at least one first MOS (102) transistor and the at least one second MOS transistor (104) and having a second residual stress level (col. 6, lines 37-51) different than the first residual stress level.

Regarding claim 14, En teaches (fig. 2I) the entire claimed structure of claim 12 above including the dielectric layer (172) includes (forming contact openings) contact openings (170) therethrough for providing electrical connection to the at least one first MOS transistor and to the at least one second MOS transistor.

Regarding claim 15, En teaches (fig. 2I) the entire claimed structure of claim 12 above including the at least one first MOS transistor comprises NMOS transistor (102) and the at least one second MOS transistor comprises PMOS transistor (104), and wherein the first (150) and second (130) layers have opposite residual stress levels (refer to col. 7, lines 50-60 and col. 6, lines 37-51).

Regarding claim 16, En teaches (fig. 2I) the entire claimed structure of claim 12 above including the first layer has a positive residual stress (tensile stress, col. 7, lines 50-60) level above the NMOS transistors, and the second layer has a negative residual stress (compressive stress, col. 6, lines 37-51) level above the PMOS transistor.

Regarding claim 19, En teaches (fig. 2I) the entire claimed structure of claim 12 above including a zone formed by the second layer overlapping the first layer (the region where the compressive stress and the tensile stress intersect, the middle region of the CMOS device) has a substantially zero residual stress level.

Regarding claim 20, En teaches (fig. 2I) a semiconductor device comprising: a semiconductor substrate (106); at least one NMOS transistor (102) and at least one PMOS transistor (104) in the semiconductor substrate; a dielectric layer (172) on the at least one NMOS transistor (102) and on the at least one PMOS transistor (104); a first layer (150) covering the at least one NMOS transistor and having a first residual stress

level (refer to col. 7, lines 50-60); and a second layer (130 and 140) covering the at least one NMOS transistor and the at least one PMOS transistor and having a second residual stress level different than the first residual stress level (col. 6, lines 37-51).

Regarding claim 22, En teaches (fig. 2I) the entire claimed structure of claim 20 above including the dielectric layer (172) includes contact openings (170) therethrough for providing electrical connection to the at least one NMOS transistor and to the at least one PMOS transistor.

Regarding claim 23, En teaches (fig. 2I) the entire claimed structure of claim 20 above including the first (150) and second (130) layers have opposite residual stress levels (refer to col. 7, lines 50-60 and col. 6, lines 37-51).

Regarding claim 24, En teaches (fig. 2I) the entire claimed structure of claim 20 above including the first layer has a positive residual stress (tensile stress, col. 7, lines 50-60) level above the at least one NMOS transistor, and the second layer has a negative residual stress (compressive stress, col. 6, lines 37-51) level above the at least one PMOS transistor.

Regarding claim 25, En teaches (fig. 2I) the entire claimed structure of claim 20 above including a zone formed by the second layer overlapping the first layer (the region where the compressive stress and the tensile stress intersect, the middle region of the CMOS device) has a substantially zero residual stress level.

4. Claims 12, 17-18, 26, 28-32, 34 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by En et al., US patent No. 6,573,172.

Regarding claims 12 and 32, En teaches (fig. 2I) a semiconductor device comprising: a semiconductor substrate (106); at least one first MOS transistor (104) and at least one second MOS transistor (102) in the semiconductor substrate; a dielectric layer (172) on the at least one first MOS transistor (104) and on the at least one second MOS transistor (102); a first layer (130) covering the at least one first MOS transistor (104) and having a first residual stress level (col. 6, lines 37-51); and a second layer (150 and 140) covering the at least one first MOS (104) transistor and the at least one second MOS transistor (102) and having a second residual stress level (refer to col. 7, lines 50-60) different than the first residual stress level. En also teaches a method for fabricating a semiconductor device (fig. 2A-2I).

Regarding claim 17, En teaches the entire claimed structure of claim 12 above including the at least one first MOS transistor comprises PMOS (104) transistors and the at least one second MOS transistor comprises NMOS (102) transistors, and wherein the first and second layers have opposite residual stress levels (refer to col. 7, lines 50-60 and col. 6, lines 37-51).

Regarding claim 18, En teaches the entire claimed structure of claim 12 above including the first layer has a negative residual stress (compressive stress, col. 6, lines 37-51) level above the PMOS transistors, and the second layer has a positive residual stress (tensile stress, col. 7, lines 50-60) level above the NMOS transistors.

Regarding claim 26, En teaches (fig. 2I) a semiconductor device comprising: a semiconductor substrate (106); at least one PMOS transistor (104) and at least one NMOS transistor (102) in the semiconductor substrate; a dielectric layer (172) on the at

least one PMOS transistor (104) and on the at least one NMOS transistor (102); a first layer (130) covering the at least one PMOS transistor (104) and having a first residual stress level (col. 6, lines 37-51); and a second layer (150 and 140) covering the at least one PMOS (104) transistor and the at least one NMOS transistor (102) and having a second residual stress level (refer to col. 7, lines 50-60) different than the first residual stress level.

Regarding claim 28, En teaches (fig. 2I) the entire claimed structure of claim 26 above including the dielectric layer (172) includes contact openings (170) therethrough for providing electrical connection to the at least one NMOS transistor and to the at least one PMOS transistor.

Regarding claim 29, En teaches (fig. 2I) the entire claimed structure of claim 26 above including the first (130) and second (150) layers have opposite residual stress levels (refer to col. 7, lines 50-60 and col. 6, lines 37-51).

Regarding claim 30, En teaches (fig. 2I) the entire claimed structure of claim 26 above including the first layer (130) has a negative residual stress (compressive stress, col. 6, lines 37-51) level above the at least one PMOS transistor, and the second layer (150) has a positive residual stress (tensile stress, col. 7, lines 50-60) level above the at least one NMOS transistor.

Regarding claim 31, En teaches (fig. 2I) the entire claimed structure of claim 26 above including a zone formed by the second layer overlapping the first layer (the region where the compressive stress and the tensile stress intersect, the middle region of the CMOS device) has a substantially zero residual stress level.

Regarding claim 34, En teaches (fig. 2I) the entire claimed structure of claim 32 above including the dielectric layer (172) includes (forming contact openings) contact openings (170) therethrough for providing electrical connection to the at least one first MOS transistor and to the at least one second MOS transistor.

Regarding claim 35, En teaches (figs. 2a-2I) the entire claimed process of claim 32 above including forming the first layer (130) covering the at least one first MOS transistor (104) and the at least one second MOS transistor (102); forming a mask (134) on the at least one first MOS transistor (104); removing the first layer (130) on the at least one second MOS transistor (102); and removing the mask (refer to figs 2B-2D).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 13, 21, 27 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over En.

En teaches (fig. 2I) substantially the entire claimed structure of claims 12, 20, 26 and 32 above except explicitly stating that the first and second layers have different thicknesses.

Parameters such as thickness and width in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device quality during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the first and second layers as claimed in the structure of En in order to improve carrier mobility.

7. Claims 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over En in view of admitted prior art (APA).

Regarding claim 36, En teaches (figs. 2a-2l) substantially the entire claimed process of claim 32 above except explicitly stating performing a localized treatment of the first and second layers that overlap the at least one first MOS transistor for modifying the second residual stress level of the second layer.

APA teaches that ion implantation is used on nitride layer to improve either improve the operation of PMOS transistor or NMOS transistor (APA, specification page 2).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the treatment suggested by APA as claimed in the process of En in order to further enhance the mobility of the MOS transistors.

The combined process of En and APA would modify the second residual stress level of the second layer.

Regarding claim 37, En teaches (figs. 2a-2l) substantially the entire claimed process of claims 32 and 36 above including performing the localized treatment comprises implanting ions into the second layer (APA, specification page 2).

Regarding claim 38, En teaches (figs. 2a-2l) substantially the entire claimed process of claims 36 and 37 above including germanium ions are implanted into the second layer (APA, specification page 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
January 28, 2005

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